

**REMARKS**

Claims 1-10 were pending in the present application. No claims have been cancelled, amended, or added. Accordingly, claims 1-10 are currently under consideration. No new matter has been added.

**Concerning the drawings**

Figures 1-12 are amended to overcome the Examiner's objections in the Office Action.

**Rejections under 35 U.S.C. §112**

The Office has rejected claims 1-10 under 35 U.S.C. §112 as allegedly failing to comply with the enablement requirement. Applicants respectfully traverse this rejection.

In response, Applicants would like to bring the Examiner's attention to the following sections of the specification. First, "the variable resistor 30 connected to the drain region 23 ... is connected to the respective bit line" (see page 26, lines 1-4), and "... the gate is connected to the word line" (see page 17, lines 7-8). One skilled in the art would be able to understand that voltages applied to the word line and the bit line at the same time would effectively represent voltages applied to both ends of the variable resistor.

From the specification of the pending application, a voltage of a prescribed polarity is applied to the bit line, and a voltage is applied to the word line, so that data is written to the one memory cell (see page 17, lines 10-15). A voltage of a polarity opposite to the prescribed polarity is applied to the bit line, and a voltage applied to the word line, so that data is erased from the one memory cell (see page 17, lines 17-23). In other words, "... the data write operation and the data erase operation are switched by merely inverting the polarity of the voltage applied to the bit line" (see page 27, lines 23-24 to page 28, lines 1-2). One skilled in the art would be able to understand from reading the specification that voltages of the same polarity applied on both ends of the variable resistor would result in data being written, while voltages of opposite polarity applied on both ends of the variable resistor would result in data being erased.

The examples disclosed on pages 26 and 27 further demonstrate this point. For writing data to the selected memory cell 10, for example,  $V_{wl} = 3.0$  V is applied to the word line and  $V_{bl} = 5.0$  V is applied to the bit line. “As a result, the resistance value of the variable resistor 30 of the selected memory cell 10 is changed from an initial state” (see page 26, lines 21-24 to page 27, lines 1-8). For erasing data from the selected memory cell 10, for example,  $V_{wl} = 3.0$  V is applied to the word line and  $V_{bl} = -5.0$  V is applied to the bit line. “As a result, the resistance value of the variable resistor 30 of the selected memory cell 10 is returned to the initial state (data erase state)” (see page 27, lines 10-21).

In other words, the resistance value of the variable resistor is changed from the initial state during the data write operation that corresponds to voltages of the same polarity applied on both ends of said resistor. The resistance value is returned to the initial state during the data erase operation that corresponds to voltages of opposite polarity applied on both ends of said resistor. One skilled in the art can appreciate from the embodiments of the present application that a reversible change in the resistance value of the variable resistor would be initiated by changing the polarity of the voltage applied to the resistor.

Therefore, the specification of the pending application teaches how the variable resistor is reversibly changed in accordance with a voltage applied thereto as recited in claims 1-10, and thus would enable one skilled in the art to make and/or use the invention.

#### **Rejections under 35 U.S.C. §103(a)**

The Office has rejected claims 1-10 under 35 U.S.C. §103(a) as allegedly being unpatentable over Hamaguchi (6,862,213).

In response, Applicants respectfully submit that Hamaguchi cannot be used as a prior art under 35 U.S.C. §103(a). According to 37 CFR 1.104(c)(4), “subject matter which is developed by another person which qualifies as prior art only under 35 U.S.C. 102(f) or (g) may be used as prior art under 35 U.S.C. 103 against a claimed invention unless the entire rights to the subject matter and the claimed invention were commonly owned by the same person or organization or subject to an

obligation of assignment to the same person or organization at the time the claimed invention was made.” (Emphasis Added)

Applicants submit that the invention disclosed in the present application and the invention disclosed in the Hamaguchi reference are commonly assigned to the same organization Sharp Kabushiki Kaisha at the time the claimed invention was made. Therefore, this rejection should be withdrawn.

### CONCLUSION

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue. If it is determined that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone the undersigned at the number given below.

In the event the U.S. Patent and Trademark office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to Deposit Account No. 03-1952 referencing docket no. 299002057400. However, the Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

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Respectfully submitted,

By 

Thomas C. Chan

Registration No.: 51,543  
MORRISON & FOERSTER LLP  
755 Page Mill Road  
Palo Alto, California 94304-1018  
(650) 813-5616

Attachments

### **AMENDMENTS TO THE DRAWINGS**

The attached sheets of drawings include changes to figures 1-12 in order to comply with the examiner's requests.

Attachment: Replacement sheets, twelve (12)